Long Island University

Notes:
The exam questions may be in different format
Memory topic will be included in the exam
The exam will have fewer questions than this review

Base Conversion:

(FA10E) 16 =(??)8

(101001)2 = (??)16
       =(??) 8
        =(??)10
(26789) 10 =(??)8
       =(??)16

Arithmetic
1. Convert the decimal number 0.625 into floating point IEEE Standard 754 single precision:

2. Perform the following binary multiplication of two binary numbers:
   10111011 and 11101101

TRUE OR FALSE

1. At a top level, a computer consists of CPU, memory, and I/O components.
2. Program execution consists of repeating the process of instruction fetch and instruction execution.
3. An I/O module cannot exchange data directly with the processor.
4. A key characteristic of a bus is that it is not a shared transmission medium.
5. The method of using the same lines for multiple purposes is known as *time multiplexing*.
6. Both sign-magnitude representation and twos complement representation use the most significant bit as a sign bit
7. With asynchronous timing the occurrence of events on the bus is determined by a clock.
8. It is extremely easy to convert between binary and hexadecimal notation.
9. A key requirement for PCIe is high capacity to support the needs of higher data rate I/O devices such as Gigabit Ethernet.

MULTIPLE CHOICE

1. The von Neumann architecture is based on which concept?
   A. data and instructions are stored in a single read-write memory
   B. the contents of this memory are addressable by location

    C. execution occurs in a sequential fashion
    D. all of the above

2. A sequence of codes or instructions is called _____.

    A. software   B. memory
    C. an interconnect   D. a register

3. A(n) _____ is generated by some condition that occurs as a result of an instruction execution.
    A. timer interrupt   B. I/O interrupt
    C. program interrupt   D. hardware failure interrupt

4. A bus that connects major computer components (processor, memory, I/O) is called a _____.
    A. system bus   B. address bus
    C. data bus   D. control bus

5. The _____ are used to designate the source or destination of the data on the data bus.
    A. system lines   B. data lines
    C. control lines   D. address lines

6. Which of the following is (are) correct?

    A. $25 = (2 \times 10^2) + (5 \times 10^1)$
    B. $289 = (2 \times 10^3) + (8 \times 10^1) + (9 \times 10^0)$
    C. $7523 = (7 \times 10^3) + (5 \times 10^2) + (2 \times 10^1) + (3 \times 10^0)$
    D. $0.628 = (6 \times 10^{-3}) + (2 \times 10^{-2}) + (8 \times 10^{-1})$

7. The TL supports which of the following address spaces?

    A. Memory
    B. I/O
    C. message
    D. all of the above

8. The QPI _____ layer is used to determine the course that a packet will traverse across the available system interconnects.

    A. link   B. protocol
   C. routing   D. physical

SHORT ANSWER

1. A _____ register specifies the address in memory for the next read or write.
2. If two numbers are added, and they are both positive or both negative, then _____ occurs if and only if the result has the opposite sign.
3. A _____ register contains the data to be written into memory or receives the data read from memory.
4. The most common classes of interrupts are: program, timer, I/O and _____.
5. A _____ is a communication pathway connecting two or more devices.
6. The _____ lines are used to control the access to and the use of the data and address lines.
7. The _____ function is needed to ensure that a sending QPI entity does not overwhelm a receiving QPI entity by sending data faster than the receiver can process the data and clear buffers for more incoming data.

Logic Gates

We wish to synthesize a 2 to 4 decoder with active outputs low.
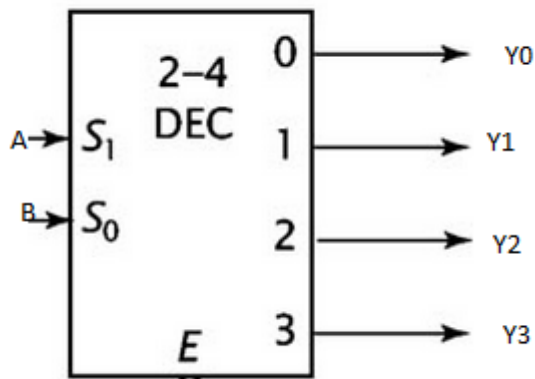
1. Establishing the truth table of the circuit.
2. Determine output functions Y= f(A,B) A and B are the i

Analyze the circuit below and define its role.

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